Remarks and Arguments

Reconsideration is respectfully requested.

Claims 14-15 are pending in the present application before this amendment. By the present amendment, claims 14-15 have been amended. No new matter has been added.

In the office action (page 2), the examiner rejects claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 7,088,797 (Momtaz et al).

The applicant thanks the examiner for the interview conducted on September 14, 2009 during which claim 14 was discussed. In the office action (page 4), it is stated that the feature of "a power down controller for determining a power down condition..." is an intended use and is not a limitation of the device. During the interview, the examiner indicated amending "a power down controller for determining..." to recite --a power down controller [[for]] determining-- clarifies that this is, in fact, a feature of the device deserving patentable weight.

Furthermore, the applicants discussed the amendment to claim 1 to recite --a clock enable signal that controls whether the memory device receives the external input clock and that is inputted to the DLL--. As discussed, this amendment clarifies the clock enable signal as well as its relation to the power down condition. The examiner indicated that claim 14, as clarified, does not appear to be taught by the prior art of record, but would require additional search and consultation which his primary examiner.

Furthermore, the applicants noted the amendment to correct a typo causing an error, so that claim 14 recites that the first clock signal is output in a non-power down condition and the second clock signal is output during a power down condition, with the first clock signal having a frequency higher that that of the second clock signal.

In claim 14, a synchronous memory device comprises:

--a delay locked loop (DLL) having a clock divider comprising a plurality of clock signal dividers connected in series,

a power down controller ~~for~~ determining a power down condition based at least on a predetermined state of a clock enable signal **that controls whether**

the memory device receives the external input clock and that is inputted to the DLL,

wherein the clock divider outputs a first clock signal being one of the output signals of the clock signal dividers excluding the last clock signal divider of the series when the synchronous memory device is in **a non-power down condition** ~~the power down condition~~,

wherein the clock divider outputs a second clock signal being an output signal of the last clock signal divider of the series when the synchronous memory device is in ~~a non-power~~ **the power** down condition, and

wherein a frequency of the first clock signal is ~~lower~~ **higher** than that of the second clock signal.--

Momtaz fails at least to disclose the clock enable signal and the power down condition of the presently claimed invention.

In the presently claimed invention, the clock enable signal (CKE) is the signal that determines whether the memory device has received an external clock signal. That is, when the clock enable signal is enabled, the memory device would receive the external clock signal; and when the clock enable signal is disabled, the memory device does not receive the external clock signals..

As clarified, claim 1 clarifies this feature: --a power down controller determining a power down condition based at least on a predetermined state of a clock enable signal that controls whether the memory device receives the external input clock and that is inputted to the DLL--.

The power down condition is a mode in which power is saved, and the power down condition is determined by the power down controller **according to the clock enable signal** (which, as claimed, controls whether the memory device receives the external input clock).

Accordingly, as claimed, based on the clock enable signal, which controls whether the device will receive the external input clock, the power down controller determines a power down condition and the clock divider outputs a first or second clock signal according to whether it is determined that the device is in power down or non-power down modes.

In contradistinction, Momtaz relates to a communications PLL circuit and thus cannot disclose the "power down" and "clock enable signal" of the memory device of the present invention.

In the office action (page 2), the add or drop signals of Momtaz are compared to the claimed clock enable signal. However, the add/drop of Momtaz is generated by detecting the number of data bits while the data input/output operations are performed, and thus it is clear that the add/drop signals of Momtaz do not control whether the an external input clock is received and are therefore unlike the claimed clock enable signal. It must therefore logically follow that that Momtaz cannot disclose a power down controller determining a power down condition based on a clock enable signal.

Accordingly, nowhere in Momtaz discloses the clock enable signal and the power down controller determining a power down condition based on this clock enable signal. For at least these reasons, the applicants respectfully submit claim 1 is allowable over the prior art of record.

Claim 15 depends from claim 14 and should be allowable for at least the same reasons as well as the addition features recited therein.

For the reasons set forth above, the applicant respectfully submits that claims 14-15 pending in this application are in condition for allowance over the cited references. Accordingly, the applicants respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of allowable subject matter.

This amendment is considered to be responsive to all points raised in the office action. Should the examiner have any remaining questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

Dated: Oct. 12, 2009

W. William Park, Reg. No. 55,523
Ladas & Parry
224 South Michigan Avenue
Chicago, Illinois 60604
(312) 427-1300